Full Custom Rail-to-Rail Self-Calibrating Comparator for Low Voltage Successive Approximation Register Analog-to-Digital Converter

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***Abstract*—The demand for low power consuming devices is increasing, particularly that of wireless sensor networks (WSN). This study aims to address this problem by designing a novel rail-to-rail comparator for SAR ADC integrated with self-calibration to null offset. In this study, rail-to-rail comparator, self-calibrating comparator, and rail-to-rail self-calibrating comparator are the circuits that will be designed, compared and analyzed. The three circuit designs were realized using the 0.18um CMOS technologyand has undergonePVT variations. The designed comparators all operate with a 1.8 V supply. In comparing and determining which circuit is the best in terms of their response, all the circuits will be compared based on six parameters to be measured thru the use of Simulation Program with Integrated Circuit Emphasis, also known as SPICE. The rail-to-rail comparator design resulted in an ICMR of 700mV. The self-calibratingcomparator design has a prominent value of 78dB for its CMRR. On the other hand, the novel rail-to-rail self-calibrating comparator design has highlighted a 5.15 V/us slew rate, with a power dissipation of only 22.40uW. A layout of the novel rail-to-rail self-calibrating comparator was also implemented which has a power dissipation 25.60uW and a slew rate of 4.16 V/us. It was found that the proposed design's key features are stable performance over wide temperature ranges from 0°C up to 49°C, high value of slew rate and low power consumption without compromising its function.**

***Index Terms*—ADC; Rail-to-Rail Comparator; Self-Calibrating Comparator; Novel Rail-to-Rail Self-Calibrating Comparator.**

I. INTRODUCTION

The Analog-to-Digital Converter (ADC) is a key component for electronic devices. Since most real world signals are in analog form, there is a need to convert these signals first for digital processing to occur. The most common types of ADCs are the sigma-delta ADCs, flash ADCs, pipeline ADCs, and Successive Approximation Register (SAR) ADCs. Among all the types mentioned, the SAR ADC features low cost, high-performance, and low-power consumption which makes this type of ADC to be put into miniature form factors necessary for present day demands. Generally, an ADC circuit is mainly composed of a Digital-to-Analog Converter (DAC), a sample and hold circuit, a logic gate, and a comparator. Comparators are commonly used in designing modern mixed signal systems. In most cases, the DAC array, together with the comparator block of the SAR ADC, consume most of the power and just like any other circuit, nonlinearities on the output are indispensable most of the time. A number of ADC techniques are cited in numerous research work to provide a means to make accurate, high speed and low voltage data acquisition systems such as Wireless Sensor Networks (WSNs) possible. Wireless sensor networks have emerged from military and heavy industrial applications. Today's WSNs are already applied to homes, work places and many others, bringing new sources of information, control and convenience to personal and professional lives. Most of the ADCs in this field are low-voltage devices which use renewable sources of energy such as solar power and the like. The overall operation of the ADC is dependent to the supply voltage and there is an increasing interest in low voltage converters which operate on 3V or less which are commonly used for battery powered applications. A number of research works have made improvements in the architecture of the ADC, modifying a specific block in order to boost performance [1-10]. As of now, the trend towards designing better SAR ADCs has given rise to lowering the supply voltage.

Nevertheless, the use of low supply voltage often results in a number of subtle ties which include limited Dynamic Range, a decrease in Signal-to-Noise Ratio (SNR) and a limited output swing. The issue regarding limited Dynamic Range and decreased SNR was addressed by designing the SAR ADC's comparator in rail-to-rail configuration. The use of a dynamic comparator with rail to rail signal swing in [1] resulted in high resolution operating at 1.8V. However, output offset errors are present in this type of configuration. A solution to this matter is to use a self-calibrating comparator [2]. In their study, Rabuske et al.[10] designed a comparator circuit which has neither pre amplifier nor current sources, thus lowering the supply voltage. A 18-step binary search was used to detect the offset error with 1 additional clock cycle for offset correction. For error calibration, it accelerates the slower branch instead of slowing down the faster branch.

In every related paper, one of the major issues regarding the use of low supply voltages for SAR ADC is that it limits

the peak input signal power, thus reducing SNR. The existing research journals have showed many efforts in trying to resolve the issue. Other existing research journals normally use Complementary Metal Oxide Semiconductor (CMOS) technology in order to achieve the desired supply voltage without compensating the overall performance. Also, the use of a dynamic comparator reduces static power consumption but at the expense of high offset error. Using rail to rail configuration solves the issue of reduced Dynamic Range, SNR and output swing but it is also susceptible to offset errors. Self-calibration turns out to be one solution to address this matter but self-calibration imposes drifting output voltages due to instantaneous changes in temperature.

This study aims to design a Rail-to-Rail Self-Calibrating Analog Comparator designed for a Successive Approximation Register Analog-to-Digital Converter operating on low supply voltages. The proposed study specifically aims to: (i) design three versions of comparator: Rail to Rail Comparator, Self-Calibrating Comparator and a novel Rail to Rail Self Calibrating Comparator under TT process, 25°C room temperature and nominal 3.3V supply; (ii) perform pre-layout simulations to compare 3 versions of comparator using Spice under PVT process; (iii) draw the layout of the best design and perform post-layout simulations. This study is conducted so that lowering the supply voltage of the SAR ADC is best achieved specifically by modifying the comparator block which also consumes most of the power.

II. Material and Methods

The aim of this research is to design a rail-to-rail self-calibrating comparator for low voltage SAR ADC application. The flow of this research is shown in Figure 1. A research of common rail-to-rail comparator, and self-calibrating comparator topologies will be conducted first followed by the research of parameters that are commonly used to measure the effectiveness of a basic comparator. Afterwards, a rail-to-rail comparator will be designed, characterized and simulated. The design and characterization will be done by finding the optimum transistor size for the design. The simulation of both comparator circuits will have six parameters that will be measured which are the input common mode range, input offset voltage, output offset voltage, common mode rejection ratio, propagation delay and power dissipation. The same will be done for the self-calibrating comparator.

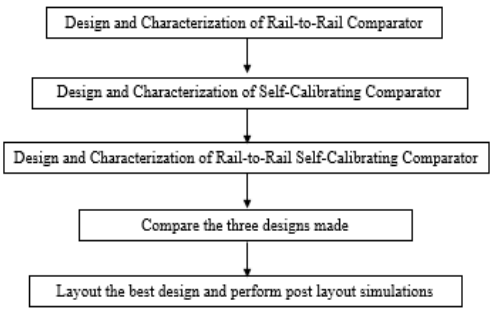

Figure 1: Conceptual Framework

A. Design of Rail-to-rail comparator

The rail-to-rail comparator has three stages, the P-differential, N-differential and the regenerative latch. The design circuit consists of 21 transistors. Figure 2 shows the schematic diagram of a Rail to Rail Comparator. For this study, the 0.18µm CMOS technology was used. The bottom-up method as well as the binning model was used in determining the sizes of the transistors. The inverters are connected tothe output nodes L1 and L2. The PMOS width for this inverter is 0.44um while the NMOS width is 0.22um. The inverters ensure that the outputs coming from nodes O1N and O1P are free from fluctuations. Table 1 shows the input parameter used.

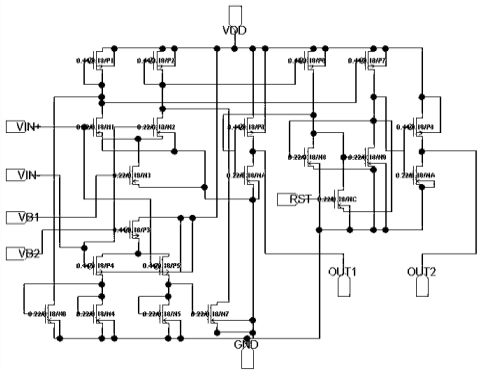

Figure 2: Schematic Diagram of a Rail-to-Rail Comparator

Table 1
Input Specifications for the Rail-to-Rail Comparator

Input Specifications	Value
Supply voltage	1.8 V
Technology	180 nm
Clock Voltage Range	0V – 1.8 V
Clock Frequency	250 Hz
Clock Rise Time	1ns
Clock Fall Time	1ns
Clock Delay	1ns
Clock Pulse Width	800um
Reference Voltage	1.1V – 2.2V

B. Design of Self-calibrating comparator

Figure 3 shows the schematic diagram of the self-calibrating comparator. For this study, the 0.18µm CMOS technology was also used. The same bottom-up method as well as the binning model was used in determining the sizes of the transistors. Unlike the rail-to-rail comparator design which has an inverter on its output. The rail-to-rail comparator design has a NOR gate instead. For this circuit, the output at nodes NO1, NO2, NO3 and NO4 are fed to NOR gates. With the same technology, the width of the PMOS used for the NOR gate is 0.44um while the width of the NMOS is 0.22u. There is also an inverter found at the output nodes 01N and 01P. The PMOS width for this inverter is 0.44um while the NMOS width is 0.22um. Other than the transistors, capacitors are also found in the Rail-to-Rail Self- Calibrating Circuit diagram. The capacitances CAL1 and CAL2 used for this particular circuit both have a value of 1pF. Table 2 shows the input parameter used.

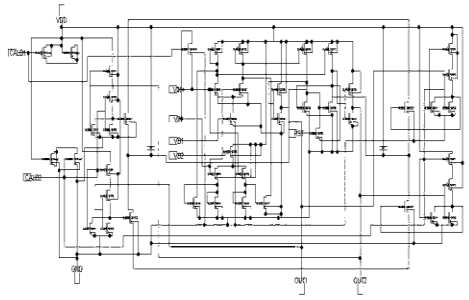

Figure 3: Schematic Diagram of the Self-Calibrating Comparator

Table 2
Input Specifications for the Self-Calibrating Comparator

Input Specifications	Value
Supply voltage	1.8 V
Technology	180 nm
Clock Voltage Range	0V – 1.8 V
Clock Frequency	250 Hz
Clock Rise Time	1ns
Clock Fall Time	1ns
Clock Delay	1ns
Clock Pulse Width	800um
Reference Voltage	0.6 V – 1.8 V
Vin+	0.9 V, sine wave at 250 Hz
Vin-	0.9V

C. Design of Rail-to-rail Self-Calibrating Comparator

The schematic of the proposed Rail-to-Rail Self-Calibrating Comparator was made by replacing the differential pair of the Self-Calibrating Comparator by Rabuske (2014) [10] with the Rail-to-Rail Comparator schematic by Kim [2] is shown in Figure 4. Since the rail-to-tail self-calibrating circuit is made by combining the schematic of the rail- to-rail and the self-calibrating comparator circuit, the sizes of the transistors that will be used is the same. Also for this circuit, the output at nodes NO1, NO2, NO3 and NO4 are fed to NOR gates. With the same technology, the width of the PMOS used for the NOR gate is 0.44um while the width of the NMOS is 0.22u. The capacitances CAL1 and CAL2 used for this particular circuit is the same as the capacitors found on objective 1.2 and they both have a value of 1pF. This value is based on existing comparator datasheets wherein 1pF is used as the load capacitance for these circuits. The calibration nodes CALB1 and CALB2 are both pulse inputs. Table 3 shows in the input settings.

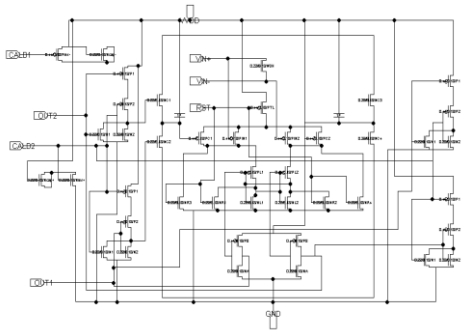

Figure 4: Schematic of the proposed Rail-to-Rail with Self-Calibration Comparator

Table 3
Input Specifications for Rail-to-Rail with Self-Calibration Comparator

Input Specifications	Value
Supply voltage	1.8 V
Technology	180 nm
Clock Voltage Range	0V – 3.3 V
Clock Frequency	25 MHz
Clock Rise Time	1ns
Clock Fall Time	1ns
Clock Delay	1ns
Clock Pulse Width	800um
Reference Voltage	0.6 V – 1.8 V
Vin+	0.9 V, sine wave at 250 Hz
Vin-	0.9V

III. RESULTS AND DISCUSSIONS

Figure 5 illustrates DC Analysis of the Rail-to-Rail Comparator. This waveform shows the inputs, Vin+ and Vin-, and the outputs VO1P and VO1N corresponding to the inputs respectively. Vin+ applied to the gate of MN1 is a ramp, sweeping from 0V to 1.8V while Vin- applied to the gate of MN2 is shorted to ground. As seen from the output, the output O1N is off before the DC sweep input crosses the DC reference voltage and turns on afterwards. The comparator is operating correctly since the outputs are alternating, meaning, when one output is at high level, the other one is at low level.

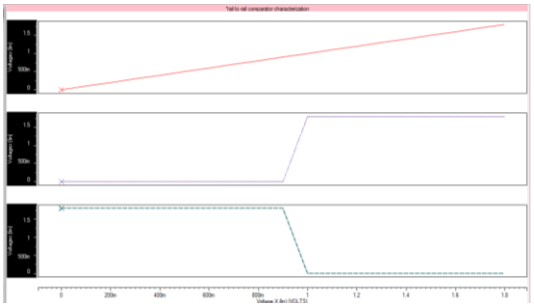

Figure 5: DC Analysis of the Rail-to-Rail Comparator

Figure 6 illustrates Transient Analysis of the Rail-to-Rail Comparator. This waveform shows the inputs, Vin+ and Vin-, and the outputs VO1P and VO1N corresponding to the inputs respectively. Vin+ applied to the gate of MN1 is a sine wave with amplitude of 1.8V and a frequency of 250 Hz, while Vin- applied to the gate of MN2 is shorted to ground. This is a normally on device, thereby explaining why the output goes back to the positive supply until the sine wave input at VIN+ crosses the reference DC voltage at VIN-.

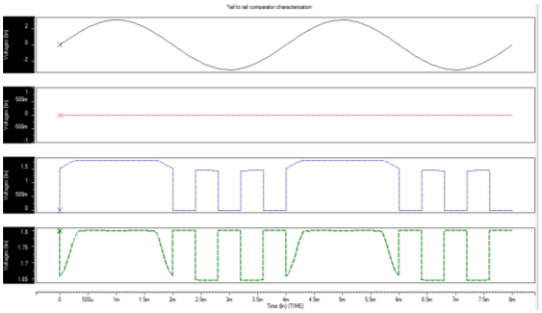

Figure 6: Transient Analysis of the Rail-to-Rail Comparator

The waveform on Figure 7 shows the supply voltage, the input Vin+, and the outputs OUT1 and OUT2 for the DC

Analysis of the Self-Calibrating Comparator. The voltage on the non-inverting terminal, Vin+, is a ramp, sweeping from 0V to 1.8V while the voltage on the inverting terminal, Vin-, is shorted to ground. As seen from the waveform, there is an evident difference between the output voltages OUT1 and OUT2 to the supply voltage. This voltage difference can be seen before calibration takes place and will be gone after calibration. Post-calibration results can be seen on the transient analysis found below.

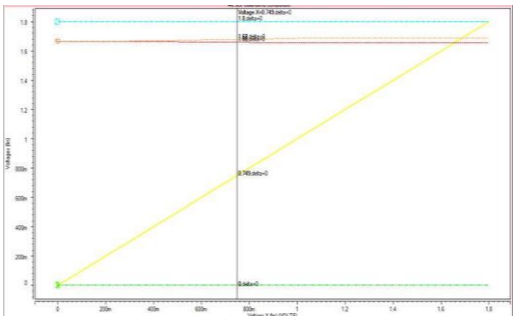

Figure 7: DC Analysis of the Self-Calibrating Comparator

Figure 8 shows the Transient Analysis of the comparator with self-calibration. To turn on the self-calibrating circuit, the non-inverting terminal of the comparator is supplied with 1.8Vdc and a sinewave at 250Hz while the inverting terminal of the comparator is grounded. The result of the comparator with self-calibration (Fig. 8) implies that fluctuation of the comparator without self-calibration was nullified, thus the output is toggling steadily between 0V and 1.8V.

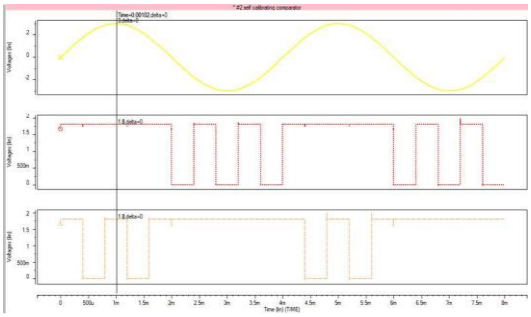

Figure 8: Transient Analysis of the Self-Calibrating Comparator

Figure 9 shows the DC analysis of the Rail-to-Rail Self-Calibrating Comparator under normal operation. The non-inverting input is fed by a ramp sweeping from 0V to 1.8V in 0.01V increment. As seen from the waveform, the output OUT1 is off before the DC sweep input crosses the half of the supply voltage, which is 09V, and turns on afterwards. The comparator is operating correctly since the outputs are alternating, meaning, when one output is at high level, the other one is at low level.

Figure 10 shows Transient analysis of the Rail-to-Rail Self-Calibrating Comparator. To minimize these fluctuations on the output, the self-calibrating circuit should be turned on. The Vin+ is supplied with 1.8Vdc and sinewave at 250Hz and Vin- = 0Vdc. The result of the graph implies that offset of the differential comparator decreased. From Figure 10, the fluctuations on the output is shows that the comparator is calibrating. At positive AC input, the circuit continuously calibrates the rail to rail comparator until it has nullified the offset voltage. At negative AC input, between -0.0715V to -.0078, the output based on the graph is digital output 0 and 1.8V

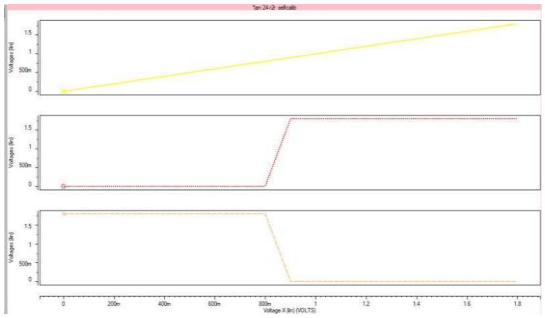

Figure 9: DC Analysis of the Rail-to-Rail Self-Calibrating Comparator.

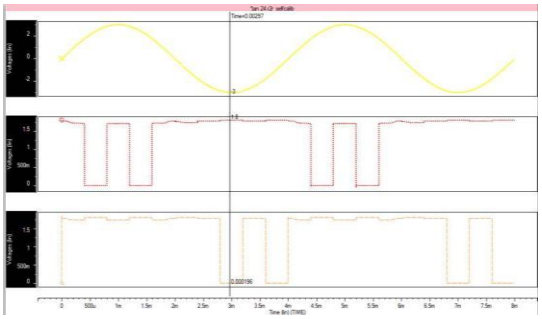

Figure 10: Transient Analysis of the Rail-to-Rail Self-Calibrating Comparator.

The comparison of all three design was done and its simulated values at TT, 25°C, 1.8V is shown in Table 4. The rail-to-rail self-calibrating comparator is defined as a circuit which nulls the offset, thereby making input offset voltage and output offset voltage measurements equal to zero after the self-calibrating process is done. The measurements for the input offset voltage and the output offset voltage shown below are made before self-calibration and without input. For this particular circuit, the simulated power dissipation and slew rate values are superior compared to the other two circuit designs made. A typical value for the power dissipation of a comparator implemented on a .18um technology is 13uW while the typical values for the slew rate is 10V/us. Other values of the parameters like the ICMR, CMRR, and Slew Rate of design 3 are in between of designs 1 and 2.

Table 4
Comparison of the three designs

Parameter	Design 1	Design 2	Design 3
(a) ICMR (mV)	700	650	670
(b) Vos (mV)	88.56	39	80
(c) CMRR (dB)	56	78	75
(d) Voo (mV)	73.34	43	77
(e) Slew Rate (V/us)	2.96	3.82	5.15
(f) Hysteresis (mV)	50	20	34
(g)Propagation Delay (ns)	49.30	27.64	100.56
(h)Power Dissipation (uW)	3.53	10.27	22.40

The Figure 11 displays the completed lay-out of the rail-to-rail self-calibrating comparator. The lay-out has a length of 185.5 microns, a width of 150 microns and an over-all area

of 27825 microns or 27.825 sq. mm. Since this study concerns analog circuits, a standard cell height is not a requirement in the lay-out unlike in digital circuits wherein a standard cell height is necessary.

After the lay-out is made, extraction will follow as based on the process flow found on the earlier part of this paper. The importance of extraction is to create an analog model of the designed circuit accurate enough that it can be said that the extracted model can emulate the actual digital and analog circuit response. For any lay-out made, lay-out extraction is a must if a Lay-out VS. Schematic (LVS) comparison will be done. A form of extraction is parasitic extraction and is defined as the calculation via simulation of the various effects of parasitics in the designed device. Parasitics include, but are not limited to, parasitic capacitances, resistances and inductances, collectively known as parasitic components.

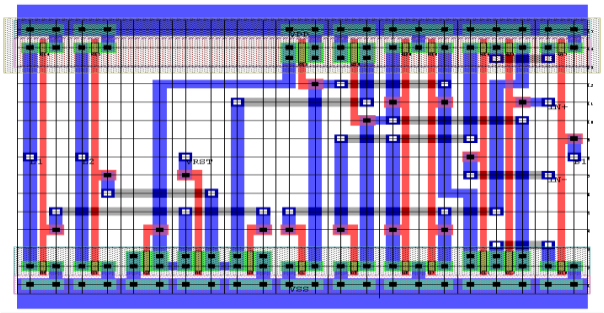

Figure 11: Final Lay-out of the Rail-to-Rail Self-Calibrating Comparator

Post-layout simulations are specifically used to verify the results of the pre-layout simulation of the completed design. As seen from Table 5, the values from the pre-layout and post- layout simulations differ slightly. Practically speaking, there are two main sources of discrepancies between the pre-layout and the post-layout measurements. The first source is modeling error and the second source is process variation. Slight variations may also be due to transistor mismatching.

Table 5
Comparison of the pre-layout and post-layout simulations of the Rail-to-Rail Self-Calibrating Comparator on TT, 25°C, 1.8V condition

Parameter	Pre-Layout Simulation Results	Post-Layout Simulation Results
(a) ICMR (mV)	670	530
(b) Vos (mV)	80	110
(c) CMRR (dB)	75	64
(d) Voo (mV)	77	92
(e) Slew Rate (V/us)	5.15	4.16
(f) Hysteresis (mV)	34	31
(g) Propagation Delay (ns)	100.56	104.93
(h) Power Dissipation (uW)	22.40	25.60

IV. CONCLUSION

This study presented the design of three comparators: the rail-to-rail comparator, the self-calibrating comparator, and the novel rail-to-rail self-calibrating comparator using HSpice 0.18µm CMOS technology. All designs have a temperature range of 0°C up to 49°C utilizinga1.8V supply voltage. Upon conducting series of trials, it can be concluded that varying the supply voltage does not affect the parameters of the circuit. This result shows that the designed comparators have a consistent performance which makes it useful for applications with varying supply voltages like automotive systems and battery-fueled electronics. Another conclusion made is that varying the temperature of the simulation has little effect on the output and on the parameters as well. From the comparisons made, the researchers conclude that the rail-to-rail comparator design has the best ICMR value of 700mV among the three designs. On the other hand, the self-calibrating comparator design has the superior CMRR, having a value of 78 dB. Although the novel rail-to-rail self-calibrating comparator design did not have the superior parameters overall, it still has the most prominent propagation delay and power dissipation of 100.56ns and 22.40uW respectively during pre-layout simulation. After the lay-out of the third design was made, a post-layout simulation was implemented and it resulted in a propagation delay and power dissipation of 104.93ns and 25.60uW, respectively. Slight variations between the pre-layout and the post-layout simulations can be attributed to modelling error and process variations.

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